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1.0 GENERAL

Comstar Corporation is dedicated to the development and design of industrial control systems using the Comstar System 4 microcomputer (CS-4). The heart of the CS-4 microcomputer is a single module Central Processor Unit (CPU) which performs all control and data processing functions. Auxiliary to the CPU is the Programmable Read Only Memory (PROM) which stores micro-programs and data tables, the Random Access Memory (RAM) for data storage, and Input/Output (I/O) modules constituting the I/O capacity of the system. The CS-4 microcomputer communicates with circuits and devices outside the family through Input/Output "ports" provided on each I/O module or out "ports" on the small RAM module.

The Programmable Read Only Memory (PROM) is programmed with a special set of microcode instructions. If the system doesn't perform according to the expectations, there may be mistakes in the programming. Since the instructions in the PROM are executed at high speed (access time 1 microsecond) and synchronously, there is no way of stopping at a particular address to check. This is where the Program Analyzer comes in. In one sentence--the Program Analyzer is useful as an aid in trouble shooting a program.

The Program Analyzer displays the process state (instruction address, instructions and data) either when the program reads a given address for the nth time ($1 \leq n \leq 16$), or when the nth external pulse is received. In other words, once the address to be checked is selected, for a given time, the Program Analyzer traps the data and Instruction at different cycle times for that selected address.

1.1 CONSOLE DESCRIPTION

The Program Analyzer (PA) does not have a built in Power Supply, hence +5 volts and ground have to be supplied. The +5 volts can be supplied either from the CS-4 microcomputer or from an external source. The Analyzer draws 1.25 amps at 5.0 volts and the user should decide whether his computer can supply +5 volts @ 1.25 amps. If the computer can supply the required power, then interconnect (1) and (3) (Figure 1.1) by using the provided cable (4). Otherwise, supply +5 and ground (GND) at (3) and (2), respectively. If the power is supplied from CS-4 microcomputer then there is no need to attach a ground connection at (2).

A 25 pin connector is provided to connect the PA input to the CPU output. The (5) in Figure 1.1 can be connected into any connector on the Data Control Bus. POINTER VALID Indicator on the console will light up when an SRC is received. Similarly DATA VALID Indicator will light up whenever the data on L.E.D.s is equal to the selected address. When DATA VALID is on, then the display values are for the desired address.

MASTER RESET and ANALYZER RESET are momentary switches. The Analyzer is initialized by pushing ANALYZER RESET or MASTER RESET. The MASTER RESET resets the CPU and the Analyzer while ANALYZER RESET resets only the Analyzer.

The advantage of ANALYZER RESET is, that the Analyzer can be reset without interrupting the program.

There are provisions for external inputs. The ENABLE switch should be set to ANALYZER ENABLE whenever External Enabling is <u>not</u> in use.

1.2 OPERATING PROCEDURE

The Program Analyzer can be operated in any of the following four modes.

1. Address Trap and Analyzer Enabled
2. Address Trap and External Enabled
3. External Trap and Analyzer Enabled
4. External Trap and External Enabled

Address Trap enables the Analyzer to trap on the selected address on the ADDRESS SWITCHES. External Trap enables the Analyzer to trap on an external signal which can be provided from EXTERNAL TRAP input. ANALYZER ENABLE position would make the Analyzer monitor the CPU immediately after the PA is initialized. On the other hand, EXTERNAL ENABLE is capable of delaying the activation of the Analyzer until an external signal is received.

Depending on the user's application of the Analyzer, one mode can be selected by placing switches at the appropriate positions. Operating procedures for all the modes are explained in Sections 1.2.1 through 1.2.4.

1.2.1 Address Trap and Analyzer Enabled

For the Program Analyzer to trap on a given address, first the address must be entered into the ADDRESS SWITCHES. The COUNT SWITCHES must be sent to n-1, where the Program Analyzer traps on the nth time, this address is executed. The TRAP switch must be set to the ADDRESS TRAP position. Since INSTRUCTION SWITCH is a momentary switch, it stays in "current" position all the time. Press the MASTER RESET switch. All indicators will flicker until the Analyzer has trapped. The DATA VALID

indicator will be on after the Analyzer has trapped. If an SRC instruction has been executed since the Analyzer was initialized, the POINTER VALID indicator will be on, and the address output by the last SRC executed will appear in the LAST POINTER indicators.

If the programmer wishes to display the address of the previous or following instruction executed, the INSTRUCTION SWITCH may be moved from its center position. Only the address will be displayed for noncurrent instructions.

1.2.2 Address Trap and External Enabled

It may be desirable to trap an address or an external signal later than the 16th time the even occurred. To permit this type of trapping, it is possible to delay the activation of the Analyzer until an external signal is received by placing the ENABLE toggle switch into the EXTERNAL ENABLE position. After the analyzer is initialized, it does not change the initial state until an external signal is received. The External signal must be TTL compatible (i.e. Logic 1: =5V and Logic 0: 0V, Sink Current 1.6 MA, Source Current 40 us). The Analyzer will begin operation when the external signal attains the logical high state. The signal must remain in the low state until the Analyzer is to be enabled.

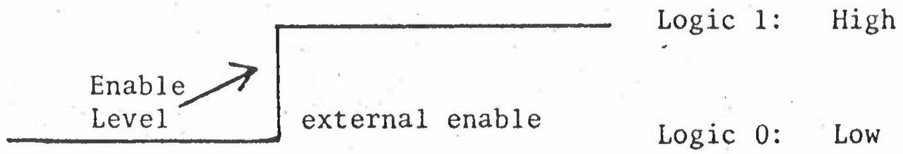


Figure 1.2.2

If the ENABLE toggle switch is not in the EXTERNAL ENABLE position, it starts monitoring the CPU immediately after it is initialized.

1.2.3 External Trap and Analyzer Enabled

If the Analyzer is to trap on the nth external input, the COUNT SWITCHES must set to n-1 and the TRAP toggle switch set to EXTERNAL TRAP before the Analyzer is initialized. The External input signal must be TTL compatible.

The Analyzer will trap on the nth time the external signal goes high, i.e.

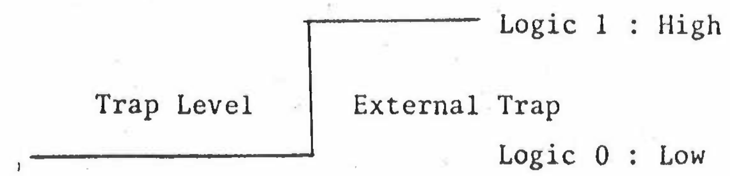


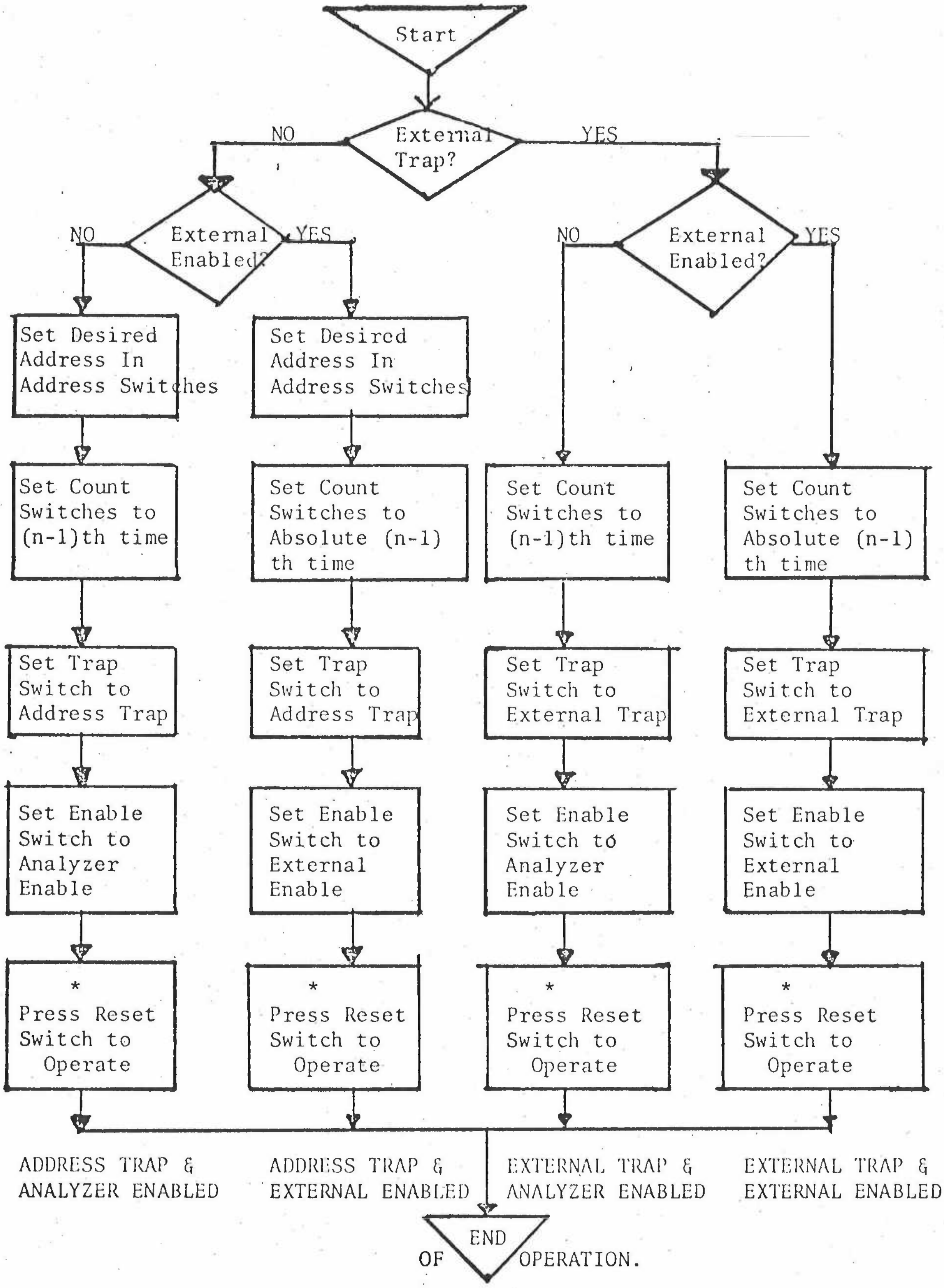
Figure 1.2.3

In this mode, the ADDRESS SWITCHES are internally disconnected.

1.2.4 External Trap and External Enabled

In some cases the user may want to see the Analyzer trap on the nth external input when n is greater than 16. This can be achieved by placing the ENABLE toggle switch into the EXTERNAL ENABLE position and the TRAP toggle switch to EXTERNAL TRAP, before initializing the Analyzer. The factors governing the response to these external inputs have already been discussed in section 1.2.3. In this mode the ADDRESS SWITCHES are internally disconnected. Regardless of the mode of operation, reset the Analyzer before operating. An additional feature of the P.A. is the ADDRESS COMPARE output. This signal is present whenever the address in the ADDRESS SWITCHES match the address of the instruction being executed. This signal may be used to trigger an oscilloscope. This signal is available as long as the Analyzer has not trapped. One means of constantly generating the signal is to load the desired address in the ADDRESS SWITCHES and choose the ADDRESS TRAP AND EXTERNAL ENABLED mode of operation. Grounding the EXTERNAL ENABLE input will then result in a permanent signal from the output ADDRESS COMPARE.

OPERATING PROCEDURE OF THE PROGRAM ANALYZER



*Master or Analyzer Reset, depending upon the progrm.
Refer to section 1.1

Figure 1.2.4

1.3 HARDWARE DESCRIPTION

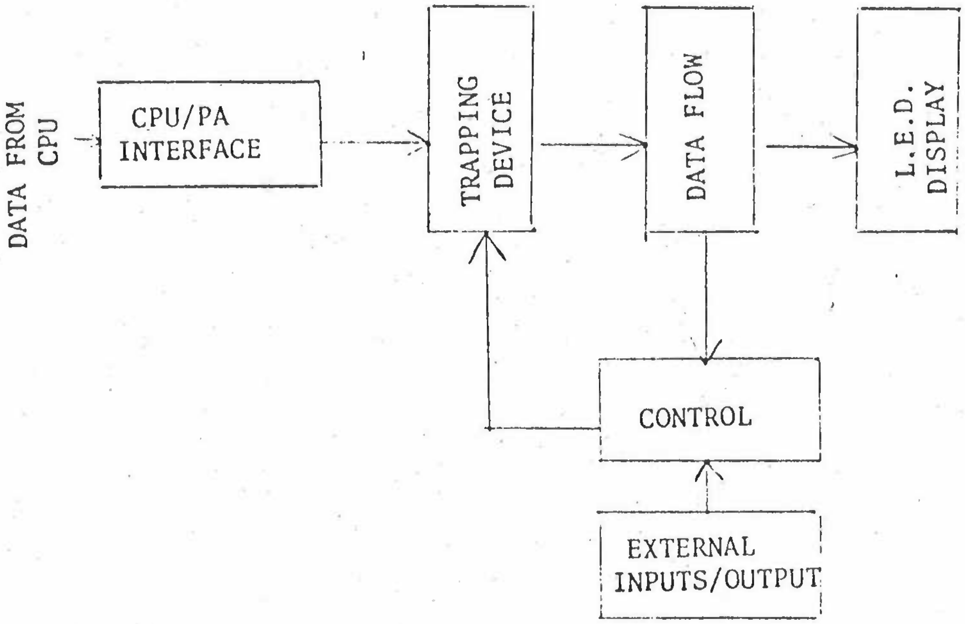


Figure 1.3 Program Analyzer Block Diagram

As shown in figure 1.3, the Program Analyzer can be divided into six blocks.

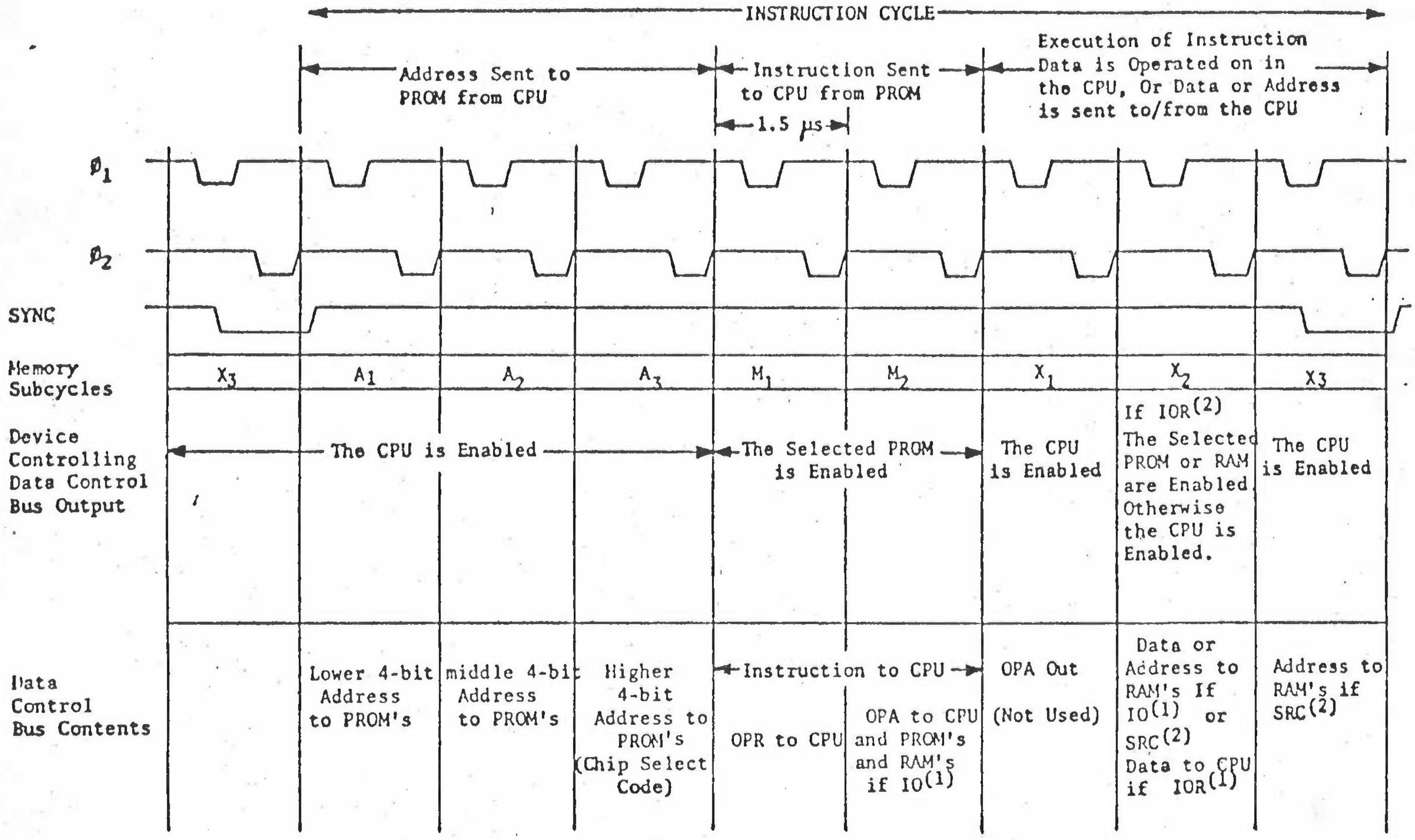
CPU/PA INTERFACE
TRAPPING DEVICE
DATA FLOW
LED DISPLAY
CONTROL
EXTERNAL INPUT/OUTPUT

1.3.1 CPU/PA Interface

The Program Analyzer is designed with TTL logic and thus requires only +5 volt level inputs. However, CPU output pins of the microcomputer are MOS voltage level (+5 and -9V). This interface block which consists if low power hex invertors, will change MOS voltage level into TTL logic level.

1.3.2 Trapping Device

The purpose of the Program Analyzer is to display data at A_1 , A_2 A_3 ,M_1 , M_2 ,X_2 and X_3 times. The basic instruction cycle of the CS4 microcomputer is shown on the next page.



(1) IO instructions control the flow of information between accumulator in CPU, I/O lines in PROM's and RAM's and RAM storage. IOR stands for IO read. In this case the CPU will receive data from RAM storage locations or I/O input lines of PROM's.

(2) The SRC instruction designates the chip number and address for a following IO instruction.

Figure 1.3.1 - BASIC INSTRUCTION CYCLE

The trapping device consists of an 8 bit serial to parallel convertor and group of AND gates.

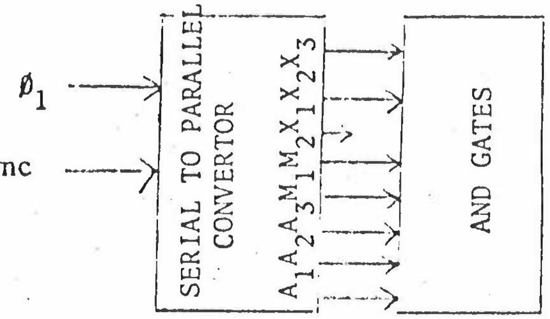


Figure 1.3.2

The serial to parallel convertor is arranged such that the A_1 position bit will have "1" and "0" in other 7 positions. Notice that X_1 is never used. When the instruction cycle is in sync, only A_1 will be out from the convertor since that is the only one assigned "1". As soon as this has happened the "1" in the A_1 position will be shifted to A_2. Thus enabling A_2 to output.

AND gates take the convertor inputs and ANDs them with the control block output (which will be explained later). The AND gates will cut off data flow once the expected output is sensed.

1.3.3 Data Flow and L.E.D. Display

The data flow block consists of all necessary connections between the trapping device and the control block. As shown in the block diagram, figure 1.3, light-emitting diodes light up according to the data. L.E.D.'s flicker until desired address is trapped.

1.3.4 External Inputs/Output and Control

External Inputs are:

Manual ADDRESS SWITCHES
Manual COUNT SWITCHES
Manual RESET SWITCHES
External pulses and other input signals on the console

External Output is: The ADDRESS COMPARE

Desired address is set with manual ADDRESS SWITCHES. Similarly, to trap on nth time, n-1 is set in the manual COUNT SWITCHES.

The control unit consists of comparators. This unit takes all external inputs and compares them with internally generated output. To be specific, three comparators compare the Address from the ADDRESS SWITCHES with the Address that has been produced at data flow stage (refer to figure 1.3). Similarly another comparator in the Control Unit compares the manually set count with an internal counter. If the addresses are equal and the counts are equal, then the Control Unit sends a command to the TRAPPING DEVICE to stop the operation.

A signal will be generated at the ADDRESS COMPARE output whenever the Address in the appropriate switches match the Address of the instruction being executed. The Analyzer can be used as a pulse generator (refer to section 1.2.4 for details).

1.4 INTERPRETING THE DATA

Each of 42 L.E.D.s on the console represents a particular operation as they light up.

LABEL	MEANING
A_1	Least significant hexidecimal digit of the address
A_2	Middle Digit
A_3	Most significant hexidecimal digit of the address
M_1	Operand Address
M_2	Operand Register
X_1	Data
X_2	Data
SRC X_2	Data at the latest SRC instruction
SRC X_3	Data at the latest SRC instruction
Pointer Valid	Will ight up when an SRC instruction is received.
Data Valid	Will light up when A_1,A_2, and A_3 match with the ADDRESS SWITCHES
Active Bank	Indicates the Bank status

NOTE: This machine has 12 ADDRESS SWITCHES (A_1,A_2,A_3 each having 4 bits). That means, one can trap up to the 4096th address (i.e. last location of the 16th PROM chip.)

A_1 A_2 A_3 M_1 and M_2 depend on the instruction address to be trapped. Hence it is easy to interpret. On the other hand, one has to have sound understanding of the program to interpret X_2 and X_3.
Each LED represents a bit. If the L.E.D. is on, it's one; if it's off it's zero. A Binary-Hexidecimal table is provided for a quick conversion.

1.4.1 Data Table

INSTRUCTIONS	DATA @ X2 $D_3D_2D_1D_0$	DATA @ X3 $D_3D_2D_1D_0$	COMMENTS
NOP	1 1 1 1	1 1 1 1	
JCN A_2 , A_1	1 1 1 1 1 1 1 1	1 1 1 1 1 1 1 1	
FIM RPO D_2 D_1	(RPO) 1 1 1 1	(RP1) 1 1 1 1	The content of address pair RP
SRC RP1	(RPO)	(RP1)	
FIN RPO 2nd cycle	(RPO) 1 1 1 1	(RP1) 1 1 1 1	
JIN RPO	(RPO)	(RP1)	
JUN A_3 A_2 A_1	A_3 A_3	1 1 1 1 1 1 1 1	
JMS A_3 A_2 A_1	A_3 A_3	1 1 1 1 1 1 1 1	
INC IR	(IR)	(IR) + 1	Content of register IR; content +1 of IR
ISZ IR A_2,A_1	(IR) 1 1 1 1	(IR) + 1 1 1 1 1	
ADD IR	(IR)	1 1 1 1	Content of register IR
SUB IR	(IR)	1 1 1 1	
LD IR	(IR)	1 1 1 1	
XCH IR	(IR)	(ACC)	Content of register IR; the Content of ACC
BBL	DDDD	1 1 1 1	Data DDDD
LDM	DDDD	1 1 1 1	Data DDDD
WRM, WRO, WR1, WR2, WR3, WPM, WMP, WRR	(ACC) (ACC)	1 1 1 1 (CY) 1 1 1 1 (CY)	Content of accumulator; content of CY F/F on D_0
RDM, RDO, RD1, RD2 RD3, ADM, SBM, RDR	(M) or (Input)	(m) or (input)	Data fetched from RAM or input
CLB, CLC, IAC, CMC CMA, RAL, PAR, TCC	0 0 0 0	1 1 1 1	
TCS	1 0 0 1	1 1 1 1	
STC, DAC, DCL	1 1 1 1	1 1 1 1	
DAA	0 0 0 0 or 0 1 1 0	1 1 1 1	X2 Depends on ACC content
KBP	0000, 0001, 0010 0011, 0100, 1111	1 1 1 1	X2 Depends on ACC content

Figure 1.4.1

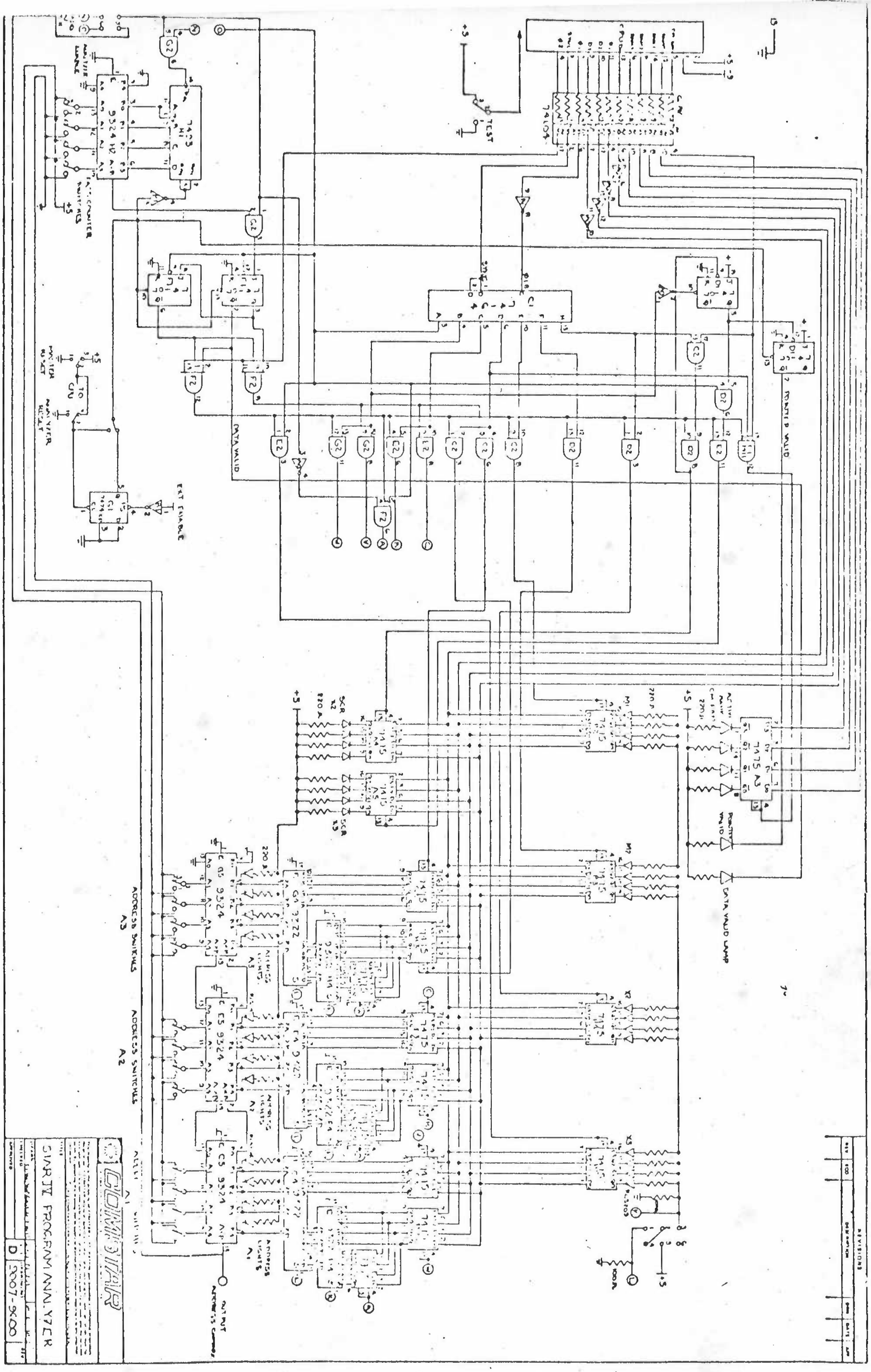
1.4.2 Binary - Hexidecimal Table

BINARY	HEXIDECIMAL
0 0 0 0	0
0 0 0 1	1
0 0 1 0	2
0 0 1 1	3
0 1 0 0	4
0 1 0 1	5
0 1 1 0	6
0 1 1 1	7
1 0 0 0	8
1 0 0 1	9
1 0 1 0	A
1 0 1 1	B
1 1 0 0	C
1 1 0 1	D
1 1 1 0	E
1 1 1 1	F

Figure 1.4.2

1.4.3 Exception

This machine cannot locate the previous address or the next address for the FIN instruction. FIN is a one-word instruction and takes two cycles to execute. This disables the Analyzer to locate the previous and the next address.



ADDRESS SWITCHES A3
ADDRESS SWITCHES A2
DATA VALID LAMP
EXT ENABLE
TEST
74175
9324

Figure 1.5